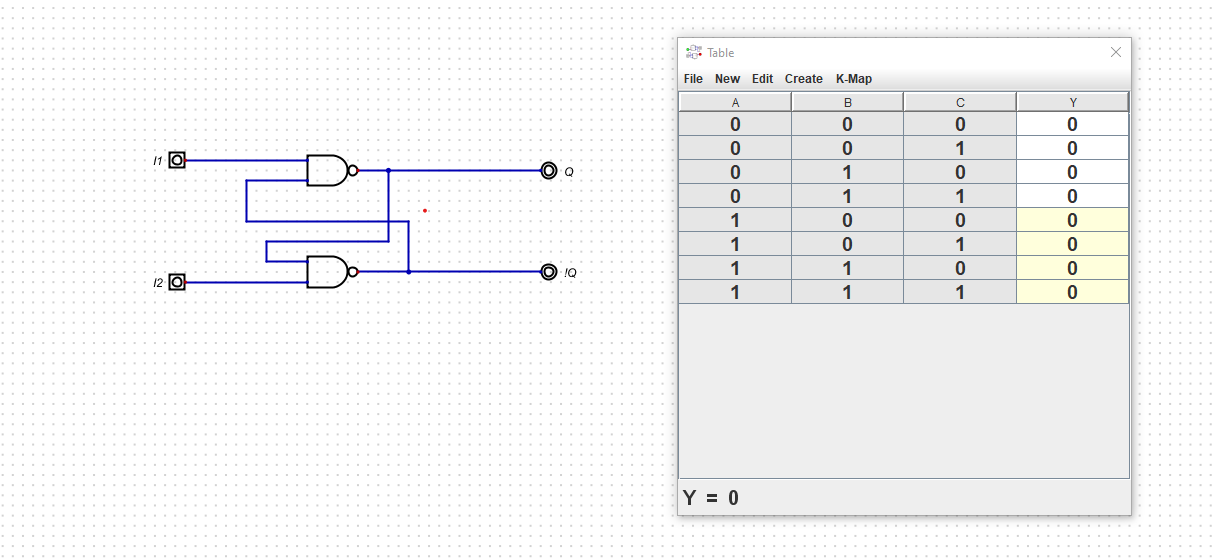
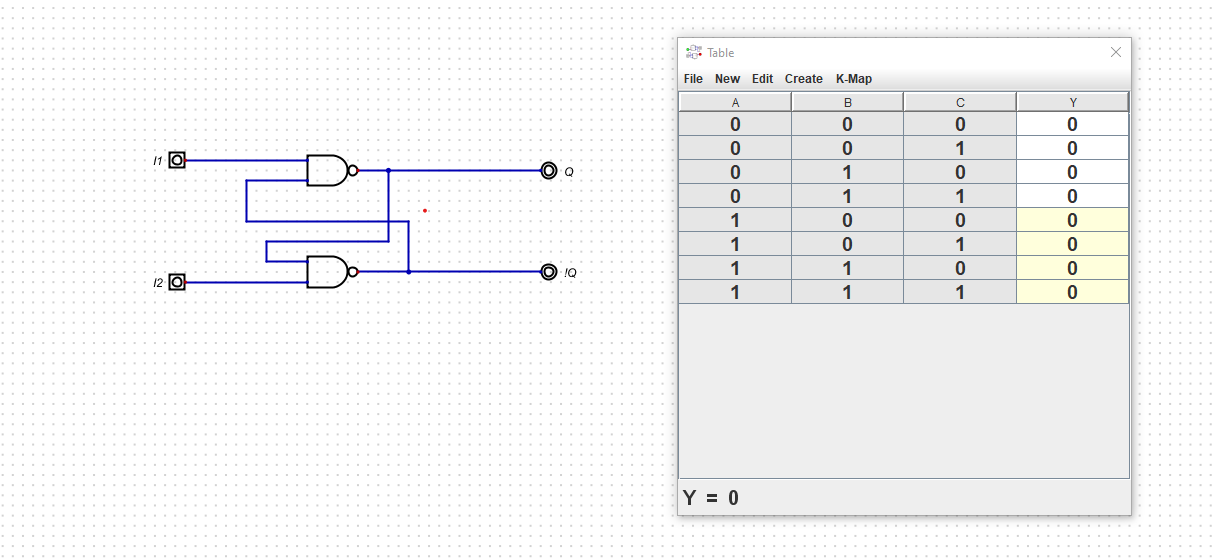
Using NAND Gates. SR Flip-Flop

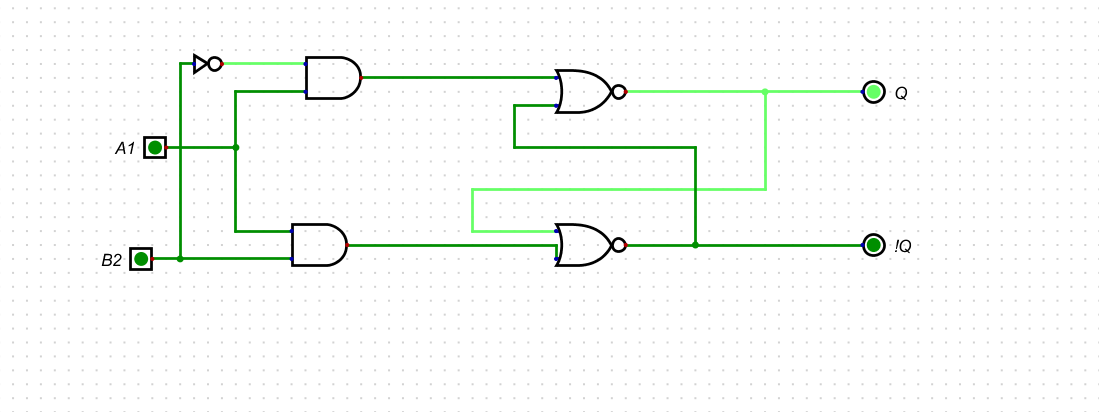


Equation for SR =>Qn+1 =S + R’Qn

Using NAND and AND Gates. Clocked SR Flip Flop



D-Latch from SR FLip Flop



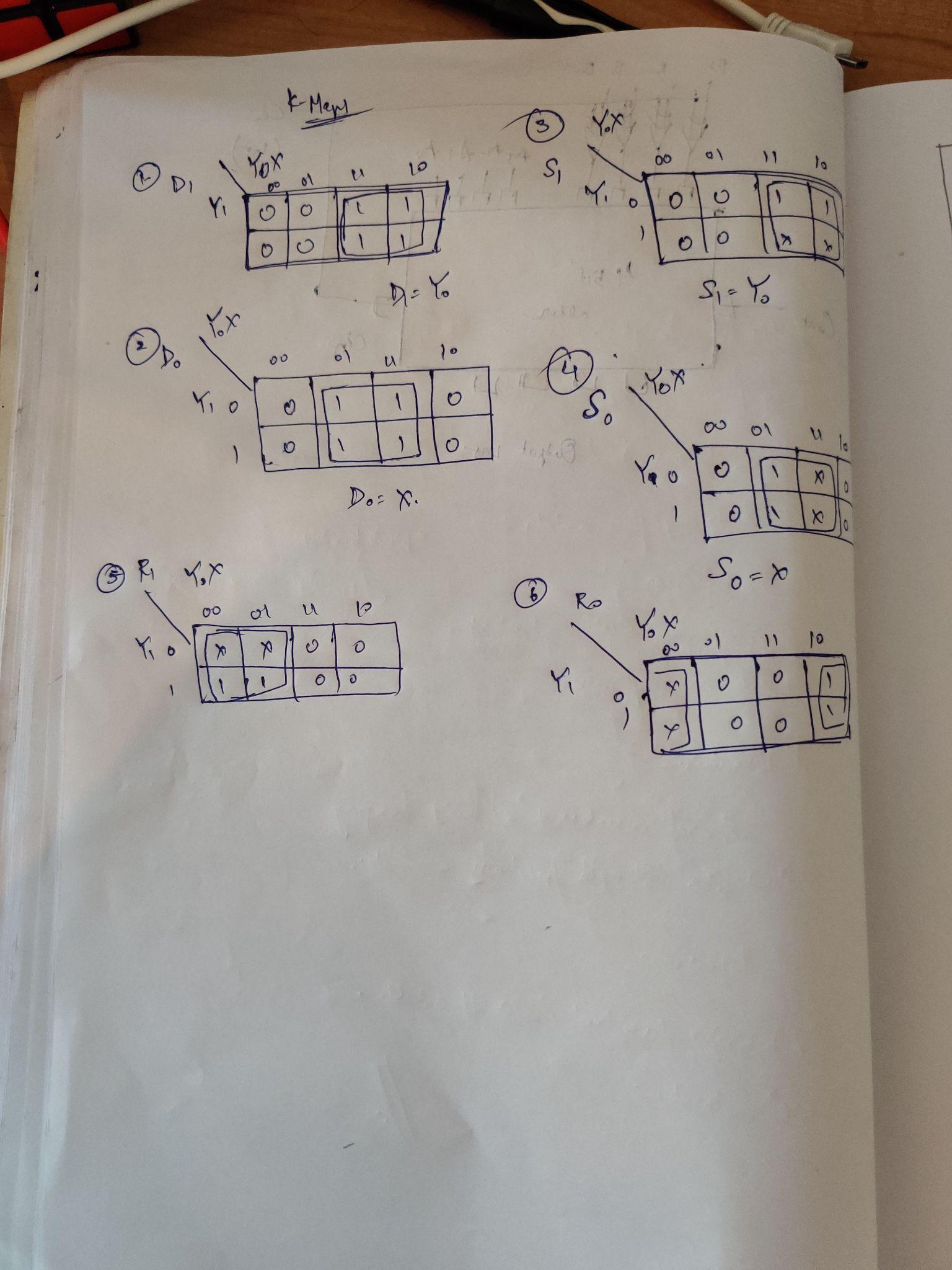
3.

| C state | x (Input) | Next state | z(output) |
| --- | --- | --- | --- |
| q0 | 0 | q1 | 0 |
| q0 | 1 | q0 | 0 |
| q1 | 0 | q3 | 0 |
| q1 | 1 | q2 | 1 |
| q2 | 0 | q1 | 0 |
| q2 | 1 | q0 | 1 |
| q3 | 0 | q3 | 0 |
| q3 | 1 | q2 | 0 |

State Encoding Table

| Y1 | Y0 | X | N1 | N0 | Z | D1 | D0 | S1 | R1 | S0 | R0 |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | X | 0 | X |
| 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | X | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | X | 0 | 0 | X |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | X | 0 | X | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | X | 0 | 0 |
| 1 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 1 |
| 1 1 | 1 1 | 0 1 | 1 1 | 0 1 | 0 0 | 1 1 | 0 1 | X X | 0 0 | 0 X | 0 1 |

K-Maps



Z =